

Design the Chip of the Future

PG Level Advanced Certification Programme in

# **VLSI Chip Designing**

For VLSI and Semiconductor professionals who want to enhance their expertise





# 4 Reasons Why This Programme is Unique

### **Get the IISc Advantage**



Designed by IISc's Electronics Systems Engineering Department



Delivered by top researchers in VLSI Design and Application



Access to VLSI Research Labs to implement projects



Get globally recognized certificate from IISc, India's #1 University



### **Outting-edge Applied Learning**



Practise on FPGA Boards with Cadence Tools



Hands on curriculum for effective learning by practitioners



Opportunity to implement your projects in state of art research labs



Industry interactions with VLSI leaders

### **⊘** Career Impact



Showcase your expertise through projects and experiments



Network with future leaders of chip design



Upgrade your technical profile with a top certification

### **Get TalentSprint Advantage**



Learn on TalentSprint's patent-pending Digital Platform



Network with 3000+ TalentSprint Deep Tech Alumni



Access TalentSprint Career Accelerator

# **About the Programme**

VLSI along with embedded software development, and hard-ware/board design is at the heart of the chip design industry. With worldwide semiconductor revenue reaching \$450 Billion in 2020, there is a need to design and produce highly efficient and specialized chips.

The PG Level Advanced Certification Programme in VLSI Chip Design enables professionals to build VLSI chip designing capabilities that can power new-age technologies like AI, IoT, VR, Mobility, Cloud, and Analytics.

The Department of Electronic Systems Engineering, IISc, with its pioneering and ongoing research and training in VLSI chip design, is best positioned to offer this programme. The programme is ideal for VLSI industry professionals who want to leverage expertise of modern tools and technologies.

The 6-month programme is delivered in a unique experiential learning process of interactive online sessions by IISc, starting from essential theoretical foundations to learning how to apply them in the real world effectively. This is accompanied by laboratory exercises using VLSI tools and boards, mentorship, case studies, and campus visits to ensure fast-track learning.



Worldwide semiconductor revenue grew to \$450 Billion in 2020, an increase of 7.3% from 2019

## **Gartner**

The Indian semiconductor manufacturing market is poised to double to over \$500 Bn by 2025

### **Business Today**



# Offered in collaboration with IISc



India's #1 University by NIRF (2016-19)



2 Bharat Ratna Awardees (1954, 2014)



Times Higher Education #1 University in India (2020)



RUR World #62 (2020)



QS Global World Ranking #185 (2020)

IISc is India's premier institution for advanced scientific and technological research and education. IISc's reputation and pre-eminence attract the finest academicians trained in the best laboratories around the world. In 2018, IISc was selected as an Institution of Eminence (IoE) by the Government of India, and it consistently figures among the top Indian institutions in world university rankings. The alumni of IISc hold significant academic and industry positions around the globe. For more information visit https://www.iisc.ac.in

The PG Level Advanced Certification Programme in VLSI Chip Design will be delivered by IISc's Department of Electronic Systems Engineering (DESE). Previously known as the Centre for Electronics Design and Technology (CEDT) it was started with support from the Department of Electronics (DoE), University Grants Commission (UGC), and Swiss Development Cooperation (SDC). DESE aims to achieve excellence in research and education in electronics systems engineering, with positive societal impact. For more information visit https://dese.iisc.ac.in/



# **Learn from Leaders**

IISc faculty members are an impressive group bearing academic vvaccreditation from premier institutions around the world

**Programme Director** 



#### Dr. Chetan Singh Thakur

Neuromorphic Computing, Mixed Signal VLSI Systems, Analog/Digital ASIC design
Ph.D., Neuromorphic Engineering, MARCS Research Institute, Western Sydney University, Australia

Assistant Professor at the Dept. of Electronic Systems Engineering (DESE), IISc. Before joining IISc, he worked as a Research Fellow at Johns Hopkins University. He has also worked with Texas Instruments, Singapore as a Sr. Integrated Circuit Design Engineer, designing IPs for mobile processors. His research interests include Neuromorphic Computing, Mixed Signal VLSI Systems, Analog/Digital ASIC design, and Machine Learning for Edge Computing.



#### **Kuruvilla Varghese**

Digital Systems, VLSI, High Performance Accelerators, Computer Networks

Principal Research Scientist at the Dept. of Electronic Systems Engineering (DESE), IISc. He has been working at DESE since 1989. Presently he is working on High performance accelerators for Machine Learning, Bioinformatics, and Networking using Field Programmable Gate Arrays (FPGA) in Reconfigurable Computing Lab at DESE. His research interests include Digital VLSI Systems and Computer Networks.



### Dr. Sanjiv Sambandan

Semiconductor Physics, Flexible Electronics

Ph.D., Electrical and Computer Engineering, University of Waterloo, Canada

Associate Professor at the Dept. of Instrumentation and Applied Physics, IISc. He is also the founder and director of Openwater, a clean water start up focused on delivering hassle-free water treatment and wastewater management solutions. Openwater is a spin-off from the Flexible Electronics Lab, IISc. He is also a lecturer at the Dept. of Engineering, University of Cambridge. His research interests includes mainly in Semiconductor Physics and Flexible Electronics.



**Dr. Arup Polley** 

Analog and Mixed Signal Design, Multi-Mode Fiber Systems

Ph.D., Electrical and Computer Engineering, Georgia Tech, USA

Associate Professor at the Dept. of Electronic Systems Engineering (DESE), IISc. Before joining IISc, he worked as a Research and Development Engineer at Kilby Labs, Texas Instruments, USA. His research interests include Analog and Mixed Signal Design, High-Performance and Multi-Mode Fiber Systems.

# Curriculum

### **⊘** Modules



#### Digital Integrated Circuit Design

- **OMOS** standard cell characteristics
- O Delay Calculation (Elmore model, Logical Effort)
- **⊘** Low Power Design
- **Static Timing Analysis**
- **O** Digital ASIC Design Flow



#### **Analog Integrated Circuit Design**

- Ø Device Physics of the MOSFET
- Physics Insights: MOSFET as a Switch
- Analytical Techniques: Low and High-frequency analysis, Noise analysis
- Ø Feedback
- **Ø** OPAMP Design
- **⊘** Oscillators and Phase-Locked Loops
- Analog Integrated Circuits Beyond Silicon



#### Advanced Digital Design and FPGA based Design

- **VLSI** Micro-architecture Design
- ∅ Timing Closure
- High Throughput Computing
- **♂** FPGA Based System Design
- Processor Design



#### **Emerging Technologies**

- **⊘** Open Source Processor Architecture (RISC-V)
- Neuromorphic Computing
- **⊘** Edge Computing
- Flexible Electronics





Cadence Analog Design Tool Suit



Xilinx Vivado



BASYS3 FPGA Board with Pmods



Digital VLSI Design Tool Suit

### **⊗** Lab Exercises



Operation Amplifier Design



ASIC Design Flow



Transient Analysis of Standard Cells



Combinational, Sequential Circuit Design



Algorithm to Architecture



Design with FPGA Boards

### **⊘** Projects



Machine Learning Accelerator for Image Classification Task



Datapath and Controller Design



And More

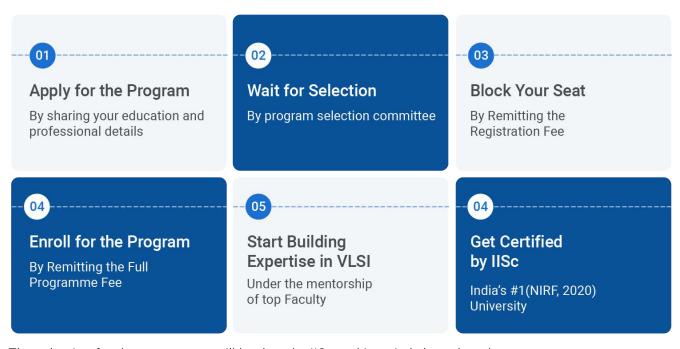
# **Delivery Format**

- Mentorship
- Hackathons
- Workshops
- Industry Interactions with Experienced Professionals
- ✓ 1 Campus Visit of 3 Days\*

# **Eligibility**

- Education: B.E./M.E./B.Tech/M.Tech or an equivalent degree
- Experience: Minimum 1 year
- Exposure: Working in VLSI domain or having VLSI working knowledge

# Your DeepTech Learning Journey



The selection for the programme will be done by IISc and is strictly based on the eligibility criteria and the motivation of applicants as expressed in their statement of purpose.

<sup>\*</sup>Dates will be decided keeping the safety of participants in mind. Fees will be based on actuals.

# **Career Accelerator**

TalentSprint's Career Accelerator offers real, tangible, and far-reaching career advancement and transformation solutions to programme participants. At TalentSprint, we are committed to helping participants connect, explore, and empower their future.



#### Compelling Profile

Build a compelling professional profile with a DeepTech edge



#### **Priority Career Access**

Get priority access to career opportunities in the industry



### **Elite Community**

Become a member of an exclusive community of DeepTech experts



### Startup Mentorship

Boost your startup ideas with professional mentorship

# **Fee with Flexible Payment Options**

Details	Domestic Participants	International Participants
Programme Fee	₹2,50,000	\$3,600
Programme Kit (FPGA Boards with Cadence Too	₹75,000	\$1,200

#### 12-Month 0% EMI Available

Fee is non-refundable and non-transferable.

Campus visit fee to be borne by participants. Will be based on actuals.

\*Upon successful enrolment, the application fee of ₹1000 (\$15) will be adjusted with the programme fee.









TalentSprint brings high-end and deep-tech education to aspiring and experienced professionals. The company's digital platform **ipearl.ai** offers a hybrid onsite/online experience to seekers of deep technology expertise. TalentSprint partners with top academic institutions such as IIT/IIM/IISc/IIITs and global corporations such as Google/Pegasystems to create and deliver world-class programs, certifications, and outcomes. TalentSprint is an NSE group company and a leading Innovation Partner for the National Skill Development Corporation, an arm of the Ministry of Skill Development and Entrepreneurship, Government of India. **www.talentsprint.com.** 





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**Programmme Partner** 



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