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To Whom It May Concern

This is a Request For Quote (RFQ) for the **procurement of chip tape-out and fabrication services** on technology nodes including but not limited to 180-nm, 130-nm, 90-nm, 65-nm, 45-nm, 22 nm CMOS and SiGe BiCMOS processes, for Analog/RF integrated circuit fabrication, as part of a limited tender for the Electrical Communication Engineering (ECE) department in IISc.

The ECE department has several research groups working on various aspects of wireless communication systems. The RF/millimeter-wave characterization laboratory in the ECE department is an initiative in IISc to explore RF circuits and systems up to 67 GHz, fabricated with commercially available semiconductor technologies such as CMOS and BiCMOS. In this context, **we invite tenders from domestic chip tapeout and fabrication service providers** to provide chip tapeout services satisfying the technical parameters specified in the table below.

Procedure:

1. Vendors will be required to submit a technical proposal and a commercial proposal in **two separate sealed envelopes**..
2. The deadline for submission of proposals is **Monday, 28th of December 2020, 5 pm**. The proposals should arrive at the office of the Department of ECE, Indian Institute of Science, India, 560012 by the above deadline.
3. The technical proposal should contain a compliance table with 4 columns in addition to the ones in the technical requirements table that has been included with this RFQ below. The compliance table should include all the items and in the same order. In addition, you should include a soft copy in MS Word ".doc" format. Please do not submit files in ".docx" formats. The first column should describe your compliance in a "Yes" or "No" response. If "No" the second column should state the extent of deviation. The "third" column should state the reasons for the deviation if any. The fourth column can be used to compare your solution with that of your competitors or provide details as requested in the technical requirements table below.
4. Items in addition to that listed in the technical table that you would like to bring to the attention of the committee can be listed at the end of the compliance table.
5. Vendors are encouraged to highlight the advantages of their solution over comparable solutions from their competitors.

	Description	Specifications
1.	**Major Application**	Chip Tapeout and Fabrication Services on CMOS/BiCMOS processes for Analog/RF integrated circuits
Basic Technical Specifications		
2.	**Process**	CMOS or SiGe BiCMOS
3.	**Node**	Including but not limited to 180-nm, 130-nm, 90-nm, 65-nm, 45-nm, 22 nm CMOS and SiGe BiCMOS
4.	**Technology Provider**	1) United Microelectronics Corporation (UMC) to ensure backward compatibility to existing designs. 2) Alternatively, a 100% Indian Manufacturer providing an RF CMOS technology at all of the technology nodes specified above.

5.	**RF CMOS Technology (basic requirements)**	1) MOS/SiGe devices providing f_T in the range of 50-500 GHz with scalable RF models based on silicon measurements. 2) High Q inductors for RF design. RF models necessary. 3) High Q MiM and MoM capacitors. RF models necessary. 4) Poly/diffusion resistors. RF models necessary.
6.	**Additional Requirements**	1) Chips will be needed for R&D. So, the die size will be in the range of 1.5x1.5 mm to 3x3 mm. Limited volumes (25 to 100 chips) are needed and so a multi-product shuttle or similar solution is desired. No high-volume fabrication is planned. 2) Should offer a minimum of 3 shuttles per year on the desired processes. 3) Must provide full PDKs of all the processes. 4) Must be able to support technical questions on process, device and circuits. 5) Must support Cadence, Mentor Graphics and Keysight ADS tools. 6) Full tapeout support. Must run all the pre-tapeout checks after LVS/DRC clean layout is provided for fabrication. 7) Must guarantee match between simulations and silicon data and provide free repeat tapeout in case it is established that fab processing errors led to problems in silicon functionality or performance.
7.	**Optional Technical Specifications**	Chip packaging support should available on QFN/QFP, Flip-chip or CSP packages.
8.	**Customer base**	Large customer base worldwide and in India. Similar solutions and support should have been provided to other customers.
9.	**Warranty & AMC**	As per norms. Free repeat tapeout should be guaranteed in case of fab processing issues leading to silicon problems.
10.	**Payment Terms**	The payment terms should be specified in the commercial proposal and is subject to negotiation.
11.	**Support**	Please provide details of the number of trained personnel in India, who can provide support in the same time zone +/- 3 HRS.
12.	**References**	Please provide references, from India and/or abroad.
13.	**Shipping**	The cost of shipping up to IISc Bangalore should be included. IISc Bangalore will help with customs clearance at Bangalore Airport. Please include your payment option.
14.	**Training**	Vendor to specify if necessary.

Thanks and best regards.

Sincerely,

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