Assistant Professor http://www.cense.iisc.ac.in/saurabh-chandorkar



## Si, SiGe and Ge Epitaxial CVD Systems

To Whom It May Concern

This is an RFQ (Request for Quote) document for procurement of an epitaxial CVD system along with attachments as part of a tender for the Centre for Nano Science and Engineering (CeNSE) at IISc, Bangalore. The CVD reactor will be primarily used to deposit thick layers of for Si, SiGe and Ge for MEMS and electronics devices.

CeNSE is a multidisciplinary research department at IISc that houses a 14,000 sq. ft. cleanroom and characterization facility used by 50 faculty members from various disciplines at IISc. CeNSE also runs a program called Indian Nanoelectronics Users Program (INUP) which has allowed 4200 participants from more than 700 universities and institutes all over India to use the facilities at CeNSE. Consequently, any tool in CeNSE receives significant exposure to scientific community at IISc and beyond. The vendors are requested to factor in the utility of this exposure in the quotes.

#### Procedure:

- 1. Vendors are required to submit a technical proposal and a commercial proposal **in two separate sealed envelopes**. Only vendors who meet the technical requirement will be considered for the commercial negotiation.
- 2. The decision of purchase committee will be final.
- 3. The technical proposal should contain a compliance table with 5 columns. The first column must list the technical requirements, in the order that they are given in the technical configuration below. The second column should describe your compliance in a "Yes" or "No" response. If "No" the third column should provide the extent of the deviation (please provide quantitative responses). The fourth column should state the reasons for the deviation, if any. The fourth column can be used to compare your tool with that of your competitors or provide details as requested in the technical requirements table below.
- 4. Any additional capabilities or technical details, that you would like to bring to the attention of the purchase committee, can be listed at the end of the technical table.
- 5. The **deadline for submission of proposals is the 26<sup>th</sup> of July 2018, 5:30 pm Indian Standard Time**. Proposals should arrive at the office of Dr. Saurabh Chandorkar, FF-08, Centre for Nano Science and Engineering, Indian Institute of Science, Bangalore 560012, India, by the above deadline.
- 6. The quotes should be CIF Bangalore, India. Please include cost of shipping.
- 7. If multiple systems can fulfill the requirements, vendors can submit multiple bids.
- 8. The technical requirements are listed for Si, SiGe, Ge epitaxy. If Si/SiGe and SiGe/Ge need separate chambers, such a configuration is acceptable as long as the combined system can share the gas manifold, pumping systems, the burnbox, and control system.

Assistant Professor http://www.cense.iisc.ac.in/saurabh-chandorkar



- 9. Please provide itemized quotes for the tool and any extra options/attachments/packages. Vendors are encouraged to quote for as many options as their tool portfolio permits.
- 10. Please indicate the warranty provided with the tool. Longer (3 year) warranty periods are preferable.
- 11. As an option, please provide cost of annual maintenance contract (AMC) for 3 years after warranty, The AMC must cover 2 scheduled and 1 emergency visit per year. It must also indicate who will service the AMC, an Indian agent or the OEM. The AMC cost must also include an itemized list of spares that are essential for the scheduled visits.
- 12. Please provide an itemized cost for spares expected over 2 years of use. These shall be used to estimate life-cycle cost of the tool.
- 13. Vendors are encouraged to highlight the advantages of their tools over comparable tools from the competitors.
- 14. Any questions or clarifications can be directed to: Dr. Saurabh Chandorkar FF-08, Centre for Nano Science and Engineering, Indian Institute of Science, Bangalore 560012
   <u>saurabhc@iisc.ac.in</u> T +91 80 2293 3638

SAURABH CHANDORKAR TE +91 80saurabhc 2293 @iisc.ac.in3638

Assistant Professor http://www.cense.iisc.ac.in/saurabh-chandorkar



# **Technical Specifications**

NNfC has a requirement for Si, SiGe, Ge epitaxy CVD system. If Si/SiGe and SiGe/Ge need separate chambers, we will prefer a common gas-manifold, load-lock, pumping system, burnbox, and control panel. If combining the two chambers is not possible, vendors can offer individual systems, either or both.

## Chamber configuration

	Si, SiGe, Ge
Chamber Temperature	Atleast 450-1200 C
Deposition Pressure	6-60 Torr
Base Pressure	50 mTorr
Deposition Rate (max)	> 0.5 um/min
	Prefer > 1 um/min
Deposition thickness during an uninterrupted run	From 50 nm to 60 um
Number of wafers/run	1
Wafer size	4". Prefer ability to do 2", 3"
	and coupons
Cleanliness	ISO Class 3 (See acceptance test
	for further specification)
Hot/Cold Walled Chamber	Cold walled strongly preferred.
	If vendor suggests hot walled
	chamber, provide justification.
Film thickness uniformity across wafer	<1%
when depositing (100%*sigma/mu)	
Film thickness variation across runs	Equal Means with alpha = 0.05
	for n = 15 runs
	Equal sigma with alpha = 0.05
	for n = 15 runs
Selective Deposition (Silicon dep on	~0 (using HCl flow, for example,
SiO2/Silicon dep on Si)	to achieve selectivity)
Matching crystal orientation from growth	100%
on single crystal	

Assistant Professor http://www.cense.lisc.ac.in/saurabh-chandorkar



Heteroepitaxy	Si on Si; Si on SiGe; SiGe on Si;
	SiGe on SiGe
Run-to-run cross contamination after	10ppm
running purge/clean recipe	
Dopant uniformity measured using sheet	<2% across
resistance measurement	
wafer (100%*sigma/mu)	

# General specifications:

	Further specification
equired Item	
Burn Box Included	Reactive
Gas panel	Required (including setup for liquid precursors)
Load lock	Required
Wafer Loading	Automatic preferred
Weight	To be specified
Size	To be specified
EMO (soft for software reset) and a	Yes
button for hard reset	
Tool status lamp	Yes
Process interlocks as per recipe	Generally: >5% deviation from set point triggers
	interlocks
Process parameter log	Every parameter sampled at ~1Hz
	Data retained for 100 runs. Logs recorded in
	chunks of
	10MB or less with appropriate
Tool log	Software log recorded in chunks of 10MB or less
Multi-step recipe creation	Control flow rates of all gasses, chamber
	pressure, temperature and other process step
	parameters
Computer interface showing current	In addition, Tool errors should be clearly
status of gas flows, chamber status,	articulated with appropriate pop up messages
load lock status etc.	as well as logged.
Tool interlock	Tool must accept external interlock so that it can

Assistant Professor http://www.cense.iisc.ac.in/saurabh-chandorkar



# Tool uptime/availability over the 95% course of a year

## **Gas Specification**

Gas		Concentration	Suggested Max Flows
			Minimum flow= 2% of
			Max
Purge	H <sub>2</sub> *	100% (5N5)	80 SLM
Purge	N <sub>2</sub> *	100% (4N8)	80 SLM
Deposition	SiH <sub>4</sub> *	100% (6N)	500 SCCM
Deposition	GeH <sub>4</sub> *	100% (5N)	50 SCCM
Deposition	$SiCl_2H_2^*$	100% (3N)	500 SCCM
Dopant	$B_2H_6*$	2% (balance 5N5 H <sub>2</sub> )	500 SCCM
		100 PPM (balance 5N5 H <sub>2</sub> )	500 SCCM
		To be diluted using H <sub>2</sub> and the	2%
		B <sub>2</sub> H <sub>6</sub>	
Dopant	PH₃*	1% (balance 5N5 H <sub>2</sub> )	500 SCCM
		100 PPM (balance H <sub>2</sub> )	500 SCCM
		To be diluted using H <sub>2</sub> and the	2%
		B <sub>2</sub> H <sub>6</sub>	
Dopant	AsH <sub>3</sub> *	100 PPM (balance 5N5 $H_2$ )	500 SCCM
Etchant for selectivity	HCI**	100% (5N)	500 SCCM
1 Extra gas line	Spare**		500 SCCM
1 extra bubbler Loop	Spare**		Implied 0.2 SCCM

\* Gases that are already available in NNfC. The concentration of these gasses is fixed.

\*\*New gas lines that need to be added. The concentration/specification of these gasses can be changed.

#### **Recipe Requirements**

- Purge/Clean recipe to remove deposition on chamber walls. Please mention the cadence at which the purge recipe must be run.
- Selective deposition on Si vs SiO2 (no deposition on SiO2) with a minimum deposited film thickness of 2um on Silicon
- Recipes for depositing 50nm, 500nm, 5um and 50um Si films
- Recipes for depositing 50nm, 500nm, 5um and 50um SiGe (50%-50%), SiGe(25%-75%), SiGe(75%-25%) films.



- Recipes for depositing 50nm, 500nm, 5um and 50um Ge films
- Recipe for thermal hydrogen annealing
- If present, robot testing functionality to carry out repeated cycle testing (picking wafer from the load lock, placing it in the chamber, retrieving the wafer from the chamber and placing it back in the load lock

#### Source Inspection

Vendors are required to send a complete hierarchical bill of materials (including mechanical, electrical, pneumatic, hydraulic parts and shipping crates) before the source inspection will be carried out. The Vendor is to notify IISc thirty (30) days in advance of factory final testing. An IISc representative may be dispatched to the Supplier for Source Inspection. The purpose of the Source Inspection is to:

- Observe testing of all ordered equipment.
- Check for equipment compliance with this specification or configuration specification.
- Check for functionality of interlocks.
- Check for manufacturing defects.

Tool aspect being tested	Test	Spec
Go over the BOM to verify presence of all components	Verify appropriate assembly of various parts in BOM	All parts should be present
Load Lock loading	25 consecutive load and unload steps in all chambers	No failures
Continuous operation of tool with no failures	5 successive recipe runs for 100 nm of Si, SiGe and Ge films	No failures
Selective Epitaxy Test	<ul> <li>i) 2µm Deposition of Epitaxial Silicon</li> <li>on a Si substrate using selective</li> <li>recipe (may need a HF dip before</li> <li>deposition at the vendor's facility)</li> <li>ii) Deposition of 2µm Epitaxial Silicon</li> <li>using selective recipe on a Si</li> <li>substrate with 250nm thermal oxide</li> <li>coating</li> </ul>	2μm deposition of Silicon substrate No Silicon deposition on SiO <sub>2</sub>
Nonselective Epitaxy Test	<ul> <li>i) 2μm Deposition of Epitaxial Silicon on a Si substrate using non-selective recipe (may need a HF dip before deposition at the vendor's facility)</li> <li>ii) Deposition of 2μm Epitaxial Silicon using non-selective recipe on a Si substrate with 250nm thermal oxide coating</li> </ul>	2µm deposition on both Silicon substrate and Silicon substrate with silicon dioxide coated on it

Assistant Professor http://www.cense.lisc.ac.in/saurabh-chandorkar



## Tool acceptance tests

Tool aspect being tested	Test	Spec
Load Lock loading	25 consecutive load and unload steps in all chambers	No failures
Continuous operation of tool with no failures	5 successive recipe runs for 100 nm of Si and SiGe films	No failures
Homoepitaxy of Si	<ul> <li>3 runs of</li> <li>1) XRD Si substrate</li> <li>2) Deposit 50nm Si</li> <li>3) Check in XRD</li> <li>4) Deposit 5um Si</li> <li>5) Check in XRD</li> <li>6) Deposit 50um Si</li> <li>7) Check in XRD</li> </ul>	<ol> <li>Match the substrate orientation</li> <li>Phi-scan to guarantee epitaxy</li> <li>Rocking curve &lt;100 arc sec</li> </ol>
Deposition uniformity (within wafer)	Test 1: Deposit 50 nm of Si, SiGe (50%-50%), Ge	9 point check; Mu/sigma <0.01 with alpha = 0.05, beta = 0.05
Deposition uniformity (across runs)	5 runs of Test 1: Deposit 50 nm of Si, SiGe (50-50), Ge each Test 2: Deposit 50 um of Si, SiGe (50-50), Ge each	9 point check (mean value to be used for each wafer) Matching means with alpha = 0.05, beta = 0.05
Cross contamination after running purge recipe	5 runs of alternating Si and SiGe runs interspaced with purge recipe	10 ppm cross contamination in films checked using XPS/EDS

SAURABH CHANDORKAR TE +91 80saurabhc 2293 @iisc.ac.in3638

Assistant Professor http://www.cense.iisc.ac.in/saurabh-chandorkar



Cleanliness test	For each film: Measure number of particles on a wafer -> Carry out 1 hour long epitaxial growth of film at the highest deposition rate, Repeat 5 times-> Measure number of added particles by comparing to be	1 particles>1um in entire wafer excluding region <=7mm from the edge of the circumference
Doping uniformity test	For each film (5 runs of): Test 1: Deposit 50nm of Si, SiGe(50-50),with 10 <sup>17</sup> /cc (split 1) and 10 <sup>19</sup> /cc doping levels (split 2) Test 2: Deposit 50um of Si, SiGe(50-50), 10 <sup>17</sup> /cc (split 1) and 10 <sup>19</sup> /cc doping levels (split 2)	9 point check for within wafer variation Mu/sigma <0.02 with alpha = 0.05, beta = 0.05 Across runs variation: Matching means with alpha = 0.05, beta = 0.05

### Other instructions

- List of required utilities must be provided by the vendor.
- Tool must be UL or CE certified
- Tool must adhere to safety code (SEMI S2-0200, SEMI S8-0999)
- Local support person is required (Must be technical support and preferably in Bangalore)
- Complete manual (hardware and software) should be provided
- Complete tool specification document including but not limited to all interlocks, complete set of circuit diagrams, top level bill of materials etc.
- Provide suitable Warranty Period (minimum of 3 years) and clear warranty terms
- Provide after warranty budget for 3 year AMC + required AMC kit/spares
- 3 references, preferably Indian, from people using this system need to be furnished with the bid
- Detailed preventive maintenance requirements and procedures are to be provided
- Include installation costs and training costs. Training can be on-site or at vendor location.
- Shipping: Bangalore CIF