E3 245 August 2 : 1

Processor System Design

Instructor

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Teaching Assistant

Email:

Department: Department of Electronic Systems Engineering

Course Time: Mon, Wed 10 - 11 AM

Lecture venue: DESE Auditorium

Detailed Course Page: http://rohini.dese.iisc.ernet.in/course/view.php?id=13 http://kuruvilla.dese.iisc.ac.in/

Announcements

First Lecture of the course E3 245 Processor System Design will be held at DESE Auditorium on Monday 7 August 2017 at 10 am

Brief description of the course

Course is about designing modern pipelined RISC processor. Course revisits the synchronization and pipelining concepts taught in prerequisites. Then the course extends the timing analysis done in prerequisite courses. After that the design of a simple multi-cycle processor is introduced. This is followed by the detailed design of a single cycle processor. Then the design of pipeline of RISC CPU is handled. Advanced topics like resolving dependancies by compiler and hardware is handled. Then students are sensitised to multiple instruction issue.

Finally BUS design is introduced. For this, basic introduction to BUS is given followed by AMBA bus is discussed, with the design of Bus interface, Bus bridges etc.

Prerequisites

Courses

E0 284 Digital VLSI design

E3 231 Digital Systems Design with FPGAs

Syllabus

Introduction:

Basic Processor Architecture, Instruction Set Design, Datapath and Controller, Timing, Pipelining.

CISC Processor Design: Architecture, hardware flowchart, implementing from flowchart, exception, control store, microcode design.

RISC Processor Design:

Single cycle implementation, multi cycle implementation, pipelined implementation, exception and hazards handling, Superscalar organization, superscalar pipeline overview, VLSI implementation of dynamic pipelines, register renaming, reservation station, re-ordering buffers, branch predictor, and dynamic instruction scheduler etc

Bus:

Bus Topologies, AMBA Bus, Bus Interface and Bridge Design, Bus Function Models, Network-on-Chip

Course outcomes

At the end of the course, a student ...

1. Given a set of specifications for a Processor, will be able to design the processor meeting the specifications.

2. In particular, given the specification, required Multi-cycle, Single-cycle or pipelined CPU would be designed. ,

3. Will be able to do the deatiled timing analysis and would be able to meet the timing requirements.

4. Will be able to resolve data dependences by stalling.

5. Will be able to solve data dependences by data forwarding and bypassing.

6. Will be able to design the bus interface for the processor

7. Will be able to design peripheral devices compatible to BUS

8. Will be able to design the BUS bridges

Grading policy

25% for the Mid term examination

25% for the Lab assignments

50% for Final examination

Assignments

All basics taught in the class are reinforced through Laboratory Exercises and culminates with a Mini project wherein a pipelined RISC processor is designed and implemented. An algorith written in C is compiled and assembly code is produced, this code is tested on the implemented design on an FPGA Board.

Resources

Computer Organization and Design: The Hardware/Software Interface, The Morgan Kaufmann Series in Computer Architecture and Design, 2011, by David A. Patterson, John L. Hennessy

Modern Processor Design: Fundamentals of Superscalar Processors, McGraw-Hill Series in Electrical and Computer Engineering by John P. Shen

Current Literature