E3 231 January 2 : 1

Digital System Design with FPGAs

Instructor

Kuruvilla Varghese
Email: kuru@iisc.ac.in

Teaching Assistant

Email:

Department: Department of Electronic Systems Engineering

Course Time: Mon, Wed 11 AM - 12 Noon

Lecture venue: DESE Auditorium

Detailed Course Page: http://rohini.dese.iisc.ernet.in/course/view.php?id=8 http://kuruvilla.dese.iisc.ac.in/

Announcements

First Lecture of the course E3 231 Digital Systems Design with FPGAs will be held held at DESE Auditorium on Monday 8 January 2018 at 11 am

Brief description of the course

Course is basically an adavanced digital system design course. The course handles how to go about implementing a digital system given the specifications of a system. In VLSI parlance, one can say it handles Front-end-design, wherein given an algorithm one can deign an architecture for it. The course handles how to design an architecture in a top-down approach for a given problem or algorithm. The course stresses a lot on Timimng Analysis to meet the timing requirement. The device technology used for the course is Field Programmable Gate Array (FPGA). Thus course handles the FPGA architecture, features of FPGA, how to design for FPGA etc. The VHDL is used for design entry for the designs in Laboratory, hence how to code for systhesis is handled in the course. Few case studies are handled in the course to learn the design of an IP.

All basics taught in the class is reinforced through Laboratory Exercises and culminates with a Mini project wherein a small Digital IP is designed and implemented by the student.

Prerequisites

Basic knowledge of Digital System Design , Digital Electronics, Microprocessors

Syllabus

Digital System Design

Introduction to Digital design; Hierarchical design, controller (FSM), case study, FSM issues, timing issues, pipelining, resource sharing, metastability, synchronization, MTBF Analysis, setup/hold time of various types of flip-flops, synchronization between multiple clock domains, reset recovery, proper resets.

VHDL:

Different models of description, simulation cycles, process, concurrent and sequential statements, loops, delay models, library, packages, functions, procedures, coding for synthesis, test bench.

FPGA:

Logic block and routing architecture, design methodology, special resources, Xilinx Spartan-6, Altera and Actel FPGAs, programming FPGA, constraints, STA, timing closure, case study.

Course outcomes

At the end of the course, a student ...

1. Given a set of specifications for a digital system, will be able to design the system meeting the specifications.

2. In particular, given an algorithm, will be able to design the datapath and the controller(s) to implement the

functionality.

3. Will be able to design datapath using higher level combinational and sequential blocks.

4. Will be able to solve the functional and timing problems in the datapath.

5. Will be able to resolve various issues related to the controller design.

6. Will be able to resolve synchronization issues.

7. Will be able to write a VHDL code to implement a particular design/block.

8. Will be able to analyze a VHDL code and infer what circuit a synthesis tool might generate out of a code.

9. Will know how the VHDL simulation tool simulates the code.

10. Will be able to write test benches to automate the verification process

11. Will be able to choose a particular FPGA for a particular application.

12. Will be able to use FPGAs in your design, meeting the area and delay constraints and estimate the power consumption.

13. Will be able to design and code to exploit the architectural features of FPGA.

Grading policy

30% for the Mid term examinations

20% for the Lab assignments

10% for Mini project

40% for Final examination

Assignments

There will be 8 Lab Assignments to reinforce what is learned in Lectures. But, the problems will not be covered in the class, this has to be learned, designed and implemented in the Laboratory. These exercises use FPGA design tool and FPGA boards.

There will be a Mini project to design and implement a Digital IP and test it on the FPGA board.

Resources

John F Wakerly, Digital Design: Principles and Practices, Prentice Hall

Kevin Skahil, VHDL For Programmable Logic, Addison Wesley.

Zainalabedin Navabi, VHDL. Analysis and Modelling of Digital Systems, McGraw-Hill

Neil H E Weste, David Harris, Ayan Banerjee, CMOS VLSI Design, Pearson Education.

Current Literature,

FPGA Data sheets