DS 397 JAN 3:1

Topics in Embedded Computing

Instructor

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Teaching Assistant

Email:

Department: Computational and Data Sciences

Course Time:

Lecture venue:

Detailed Course Page:

Announcements

Brief description of the course

This course is meant to prepare students for pursuing research on design and optimisation of runtime reconfigurable, massively parallel, many core architectures as a System-on-a-Chip (SoC).

Prerequisites

Basic knowledge of digital electronics, computer organization and design, computer architecture, data structures and algorithms, and consent of instructor.

Syllabus

Introduction to embedded processing, dataflow architectures, architecture of embedded SoC platforms, dataflow process networks, compiling techniques/optimizations for stream processing, architecture of runtime reconfigurable SoC platforms, simulation, design space exploration and synthesis of applications on runtime reconfigurable SoC platforms, additional topics including but not limited to computation models for coarse grain reconfigurable architectures (CGRA), readings and case study of REDEFINE architecture, compiler back-ends for CGRAs

Course outcomes

Many Core Architectures for SoCs

Programming massively parallel and runtime reconfigurable systems

Programming Models

Execution Models

Grading policy

Project - 60%

Assignments - 40%

Assignments

Resources